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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,732	07/30/2004	Ko-Hsing Chang	13041-US-PA	4731

31561 7590 06/14/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
HARRISON, MONICA D	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,732	CHANG ET AL.	
	Examiner	Art Unit	
	Monica D. Harrison	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/30/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Rhodes 6,856,001 B2).

2, Regarding claim 1, Rhodes discloses a method of fabricating a photodiode (Figure 10, reference 92b), comprising the steps of: providing a substrate (Figure 1, reference 12); forming a well region of a first conductive type in the substrate (Figure 1, reference 13); forming an isolation structure in the substrate to define a photosensitive area on the substrate (Figure 9, references 46A and 46B); forming a plurality of trenches in the well region of the substrate within the photosensitive area (Figure 2, reference 22; column 5, lines 27-33); and forming a doped layer of a second conductive type over the substrate, wherein the doped layer covers the interior walls of the trenches and the surface of the substrate within the photosensitive area (Figure 9, references 52 and 53).

3. Regarding claim 2, Rhodes discloses wherein forming the doped layer comprises performing an annealing operation (column 5, lines 27-33).

4. Regarding claim 3, Rhodes discloses wherein the annealing operation drives the dopants within the doped layer of the second conductive type into the substrate and makes junction of the first conductive type and the second conductive type shift into the substrate (column 5, lines 8-33).

5. Regarding claim 4, Rhodes discloses wherein the first conductive type is P-type (Figure 1, reference 13) and the second conductive type is N- type (Figure 1, reference 26).

6. Regarding claim 5, Rhodes discloses wherein the first conductive type is N-type (Figure 1, reference 13) and the second conductive type is P-type (Figure 1, reference 26; column 3, lines 25-40).

7. Regarding claim 6, Rhodes discloses wherein the step of forming the doped layer comprises performing a chemical vapor deposition process (column 3, lines 57-65).

8. Regarding claim 7, Rhodes discloses wherein material constituting the doped layer is selected from the group consisting of doped polysilicon and doped epitaxial silicon (Figure 9, reference 54).

9. Regarding claim 8, Rhodes discloses wherein the doped layer completely fills the trenches (Figure 9, reference 54).

10. Regarding claim 9, Rhodes discloses wherein the method further comprises forming a buffer layer over the substrate covering the interior walls of the trenches as well as the surface of the substrate within the photosensitive area after forming the trenches in the substrate within the photoensitive area (Figure 1, reference 14).

11. Regarding claim 10, Rhodes discloses Rhodes discloses wherein the step of forming the buffer layer comprises performing a chemical vapor deposition process (column 3, lines 41-42).

12. Regarding claim 11, Rhodes discloses wherein material constituting the buffer layer is selected from the group consisting of polysilicon and epitaxial silicon (Figure 9, reference 54).

13. Regarding claim 12, Rhodes discloses wherein after forming the doped layer over the substrate further comprises performing an annealing operation (column 5, lines 27-33).

14. Regarding claim 13, Rhodes discloses wherein the annealing operation drives the dopants within the doped layer into the buffer layer so that a junction of the second conductivity type and the first conductive type is formed within the buffer layer (column 5, lines 8-33).

15. Regarding claim 14, Rhodes discloses wherein the annealing operation drives the dopants within the doped layer into the substrate so that a junction of the second conductive type and the first conductive type is formed within the substrate (column 5, lines 8-33).

16. Regarding claim 15, Rhodes discloses wherein the doped layer completely fills the trenches (Figure 9, reference 54).

17. Regarding claim 16, Rhodes discloses a method of fabricating a photodiode (Figure 10, reference 92b), comprising the steps of: providing a substrate (Figure 1, reference 12; forming a well region of a first conductive type in the substrate (Figure 1, reference 13); forming an isolation structure in the well region of the substrate to define a photosensitive area on the substrate (Figure 9, references 46A and 46B); forming a plurality of trenches in the substrate within the photosensitive area (Figure 2, reference 22; column 3, lines 49-51); forming a buffer

layer over the substrate, wherein the buffer layer covers the interior walls of the trenches and the surface of the substrate within the photosensitive area (Figure 1, reference 14); forming a doped layer of a second conductive type over the buffer layer (Figure 9, reference 54); and performing an annealing operation to drive dopants within the doped layer into the buffer layer and form a junction of the second conductive type and the first conductive type within the buffer layer (column 5, lines 27-33).

18. Regarding claim 17, Rhodes discloses performing a chemical vapor deposition process (Figure 4, reference 34). 1

19. Regarding claim 18, Rhodes discloses wherein material constituting the doped layer is selected from the group consisting doped polysilicon and doped epitaxial silicon.

20. Regarding claim 19, Rhodes discloses wherein the step of forming the buffer layer further comprises performing a chemical vapor deposition process (column 5, lines 27-33).

21. Regarding claim 20, Rhodes discloses wherein material constituting the buffer layer is selected from the group consisting of polysilicon and epitaxial silicon (Figure 9, reference 54).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is 571-272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Monica D. Harrison
AU 2813

mdh
June 10, 2005

Craig A. Thompson

CRAIG A. THOMPSON
PRIMARY EXAMINER